Passive CMOS Single Photon Avalanche Diode Imager for a Gun Muzzle Flash Detection System

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Abstract—**We present the architecture and design of a novel 64 × 64 CMOS single-photon avalanche diode (SPAD)-based imager for gun muzzle flash detection. The imager is fabricated in a standard front side illuminated 0.18 μm CMOS image sensor process. Each pixel comprises a 25 μm diameter SPAD, a variable-load passive quenching circuit implemented with 1.8 V PMOS, an 8-bit counter, an 8-bit latch register, and digital processing electronics, and feeds an 8-bit output bus. The array delivers two-dimensional intensity data through photon counting, with integration time as low as 5 μs over the full dynamic range. Per-pixel digital memory enables fully parallel processing and global-shutter mode readout. The imager can acquire fast optical events at high frame rate (up to 200 kfps) and at single-photon sensitivity. The imager has an 8-pixel (64-bit) parallel output bus. This imager enables for the first time the detection and arrival-direction determination of individual muzzle flashes in real time, and even in the case of bursts of flashes, at a moderate cost and size. The presented results confirm the feasibility of gun muzzle flash online detection in the visible or NIR spectrum by uncooled silicon SPAD detectors using standard CMOS technology.**

Index Terms—**2-D imager, CMOS single-photon avalanche diode (SPAD), quenching, read-out, gun muzzle flash, photon counting.**

I. INTRODUCTION

IN RECENT years, significant progress has been made in the development of CMOS-based imaging arrays for very weak optical signals [1]–[4]. Extra-sensitive CMOS imagers are now able to detect even single photons [5]–[7]. Such arrays introduce a paradigm shift to photography, and enable new applications that are not implementable with conventional CMOS Image Sensors (CIS) [8]–[11]. Low-light imaging by either CMOS Single Photon Avalanche Diodes (SPAD) or CIS is continuously improving due to ongoing reductions in pixel size and noise floor [12]–[15]. CMOS SPAD arrays and CIS Figures of Merit (FoM) have been extensively reported [16], [17]. There are nowadays many applications in which single photon detection is required; the most popular among them are medical [18], [19], bio-imaging[20]–[22], fiber optic and visible light communications [23], [24]. SPAD sensors are the fastest and most sensitive silicon-based solid-state optical sensors, and in imaging applications they are used mainly for Time of Flight (TOF) measurements due to their unique timing characteristics [25], [26]. The simplest description of a SPAD is a binary photon-activated "switch" employing the avalanche mechanism. The photon-counting resolution is determined by its dead time (typically 10-20 ns). This process results in a non-linear device generating a digital rail-to-rail pulse upon detection of a photon, and can be regarded as a detector with a 1-bit analog-to-digital converter (ADC) per pixel. By digitally counting the arrivals of single photons over a chosen time interval ("frame"), recording the counter value at the end of a frame and immediately resetting it, the sequence of counter samples represents the light intensity (photon arrival rate) in each time frame, yielding a linear multi-bit ADC with one sample per frame.

In this work, we describe how the evolving technology of SPAD imagers, produced in 0.18 μm CMOS technology, can be harnessed to create a pioneering imager whose unique application is the detection of gun shots. The purpose of such an imager is to allow the rapid detection of hostile armed insurgents in combat fields, in both open and urban areas. The combination of small size, low weight, power and cost with the ability to provide high performance renders this type of imager superior over all other types of available gunshot detection technologies, including acoustical sensors, cooled infrared image sensors and microbolometer image sensors. A detailed explanations and comparisons between all sensors mentioned above can be found in references [27]–[29]. Emerging single-photon imaging technologies may be used for this application based on the detection of photons emitted by excited alkali atoms. These atoms emit photons at very specific wavelengths, which may be detected using single-photon detectors, hence overcoming many false alarms caused by solar reflections in the visual and near-infrared spectra [30]–[32].

As in any imager design, several challenges and tradeoffs should be addressed in order to ensure the imager's suitability for its exact purpose. In the case under study, the goal of the imager is to detect weak and fast optical signals in highly illuminated environments (i.e. outdoors on a sunny day), hence requiring strict optical filtering of incoming radiation and relatively short frame times. The field experiment setup including the main components is depicted in Figure 1 (a). An optical diagram of the experimental system is depicted in Figure 1 (b).
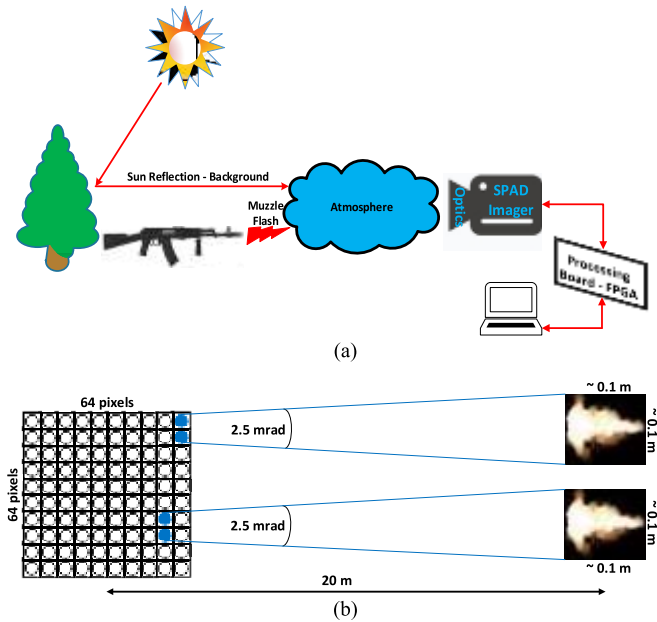
Fig. 1.   A setup of the conducted firing experiment (a) the main system components, (b) an optical diagram of the experimental system.

The aforementioned goal also determines some of the image sensor's specifications, as will be described throughout this paper. In the next sections, we describe the system concept and chip design considerations for a 64 × 64 SPADs imager prototype based on a cost-effective 0.18 μm CMOS technology. It is able to process light intensity information at pixel granularity, yielding spatial data required for the gun muzzle flash detection and imaging [29], [33]–[35]. The rest of the paper is organized as follows – section II addresses system considerations, including the preference of SPAD over highly sensitive CIS for the case under study, section III describes the different SPAD architecture considerations and the design of the imager chip, section IV describes the full system in which the imager was integrated, and section V offers concluding remarks.

II. SYSTEM CONSIDERATIONS LEADING TO SPAD IMAGER

A. Choice of Imager Sensor Technology

The gun muzzle flash detection systems in the visible or near-infrared spectrum, working in silicon-responsive wavelengths, require further development and are still not present on the market. The main challenge in this detection approach is overcoming the false alarms and background clutter caused by reflections of solar radiation, which is at its peak in this spectrum. The principle of gun muzzle flash detection in this waveband is based on the potassium nitrate wavelength doublet (766 nm and 769 nm) or sodium sulfate (589 nm) spectral emissions. For a detailed description of the detection principle, see [27]–[29], [33], [36].

Before designing the chosen image sensor architecture, two alternative sensing technologies were considered in the context of the particular application described above: SPAD, and sensitive CIS. It was concluded that between these two technologies, the preferred one for gunshot detection is a SPAD based imager. This conclusion is explained below.

The three main requirements of this application that define the properties of the desired image sensors are the sensor's frame time (which determines the sensor's read-out bandwidth, noise, fill factor and signal-to-noise ratio), the signal and background photon rates (which affect the dynamic range, saturation level, linearity, signal-to-noise ratio and fill factor) and the sensor's overall power consumption.

Although experimentally-implemented CIS chips, or quanta CIS, have nearly achieved single photon counting capabilities [5], [6], commercial CIS imagers still do not possess this ability. Also, single photon counting in CIS becomes possible at the expense of a limited full well capacity [5], [6], causing the CIS to reach their saturation level very fast (in micro-second time frames) in highly sun-illuminated environments.

In contrast, a SPAD sensor "resets" itself following each photon arrival event, and this "dead time" is on the order of 10-20 ns. Each such event causes a counter to increment the arriving-photon count. Therefore, a SPAD imager can count, per array element, photons arriving at a rate of $\sim 10^7$-10^8 photons/s. This rate is higher than the signal and background's photon rates in the application, even in sunny day conditions, since the imager is equipped with a very narrowband optical filter corresponding to the emission line of potassium.

In a CIS, the sensor resets its photodiode once per frame, during the readout process, and only then. During the reset interval the CIS is "blind". There is thus a direct coupling between the frame rate and properties of the CIS sensor itself.

In contrast, as was already pointed out, in the SPAD image sensors the quenching process (and dead times) occurs after each avalanche event. Consequently, the periods during which the sensor cannot detect photons are temporally distributed in the frame time. At the end of each time frame, all that takes place is copying of the counter value to memory (if the selected architecture is memory-based) and resetting of the counter, both of which take very few nanoseconds. In this sense, a SPAD image sensor possesses an advantage over a CMOS image sensor, because the fact that the sensor is not "blind" for one long period of time in each frame increases the chances that temporally short events occurring during a specific frame will be detected, as long as they last more than the duration of a single dead time.

Nonlinearity is another factor that affects CIS performance [37]. The digital CMOS SPAD pixel, in contrast, works on a different principle, whereby single photons are counted. Since there is no analog read-out and ADC, the CMOS SPAD pixel is practically immune to this kind of non-linearity.

Another phenomenon that is non-existent in SPAD-based imagers, due to their digital nature, is dissipation of DC power.

With respect to fill factor (FF), the SPAD's main limiting factor is a low pixel FF due to the inherently large detector area and larger amount of required auxiliary electronics. It is not expected that CMOS SPAD pixels will be scaled down to the same degree as CMOS image sensor pixels. On the other hand, since gunshot detection should be done in large fields of view due to the unknown direction of the source, this issue is less relevant for this application. Moreover, good design

of the optics may prevent degradation of the precision of the estimate of the gun's direction. The combination of the above indicates that a relatively large pixel, covering a relatively large area in the scene, is acceptable and allows implementation of an optical system with an adequate optical focal length. In contrast, very small pixels, which are typical for CIS, would perhaps allow a better FF but would also require very small optical focal length (<1mm), which would not necessarily be easy to implement.

The feasibility of gun muzzle flash detection by means of commercial SPAD and CIS has been studied in [29]. A main conclusion from the work reported there is the inherent advantage of SPAD sensors in gun muzzle flash detection mainly due to the elimination of read-out noise, which adversely affects system performance (in addition to background noise).

B. Imager Module Specifications

The detection module includes three main components – the SPAD imager comprising a 64 × 64 array of SPAD sensors, each with its own photon counter and memory, the optics and the signal processing board. The specific imager prototype has a (total for the entire array) field of view (FOV) of 9° × 9° when attached to the system's optics. The crucial system parameters, that were used for designing the imager (i.e. the signal and background photon rates, the optimal frame time and temporal duration of the shot's signal) were obtained via field experiments, as described in [27]–[29].

Based on the experimental results, it can be concluded that during a frame time of 67 μs (15 kHz sampling frequency), the average combined count of the signal and background events is predicted to be up to 110 photons per frame, for the imager under study. This number is obtained by (and dependent on) known experimental system parameters – distance, overall photon detection efficiency, optics' lens aperture diameter, dimensions and temperature of the muzzle flash and the area of the pixel under study.

The expected average photon count during the frame time dictates the in-pixel counter depth. A margin of twice the count number seems reasonable for the counter implementation. This consideration brings us to an 8-bit counter as a good compromise between dynamic range and the array's fill factor.

III. IMAGER ARCHITECTURE AND CHIP DESIGN

A. Array Organization

Several SPAD array architectures were considered:

1) 1-D Array: This enables implementation of the pixel circuits outside the pixel, thereby enabling a higher FF. However, this approach requires optical or mechanical scanning in order to create 2-D images. Such scanning can very adversely affect the system's reliability, and is thus impractical in the case under study.

2) 2-D Arrays: These create 2-D images directly, but require a more complex pixel design, at the expense of FF. Photon-counting 2-D arrays can be distinguished from one another by the existence (or non-existence) of in-pixel memory. In-pixel memory enables the storage of multi-photon events in a single frame time; the ability to count photons
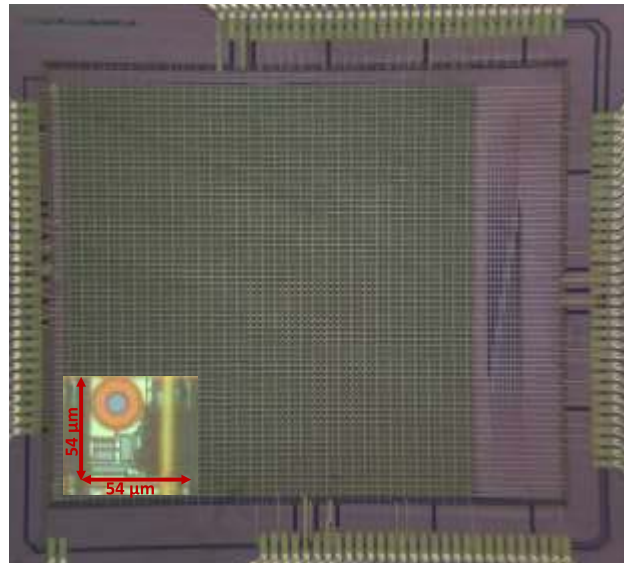

Fig. 2. The optical image of the tested chip.

during effectively longer frame times mitigates the read-out speed requirements [38]. In other words, when the pixel includes an in-pixel memory, the read-out and counting can be executed independently, in consecutive frames, but at the expense of FF. This enables fully parallel data processing (namely an "integrate-while-read" architecture) and global shutter mode readout. The convenience in this fully-parallel architecture was the main consideration for choosing a 2-D imager architecture, with in-pixel memories, as the architecture for the case under study.

B. The SPAD Imager Chip

Our SPAD based 64 × 64 pixel imager is depicted in Figure 2. The full chip size is 5 mm × 5.5 mm. The pixel size is 54 μm × 54 μm. The pixel array is located in the center of the layout. The auxiliary electronics (located in the chip peripheries) includes decoders, multiplexers and input/output drivers. The 64-bit (8-pixel parallel) output bus was implemented as well. This bus was implemented due to the impracticality of reading out all rows in parallel in this prototype chip. This impracticality arises from the layout routing density, the large number of pads that would be required and in order to allow compatibility of the readout interface to the FPGA in use. It should be noted that the all-row parallel readout interface does not reduce the frame acquisition time because the data would have to be serialized inside the FPGA in any case, in order to stay compatible with the FPGA's interface. The pin-out of the matrix is 127 pins: 11 input logic control pins (column and row scanning, global "RESET" and "LATCH" signals), 64 output pins (8 pixels in parallel), 1 pin is used for global quenching transistors' control, 32 pins are for power supplies and grounds which are distributed all over the chip. The remaining 19 pins include the temperature sensors' supply, controls and test points.

The array described herein is meant to be a prototype test chip. The array was used for proving the gunshot detection concept. The array is scalable to larger imager formats, up to
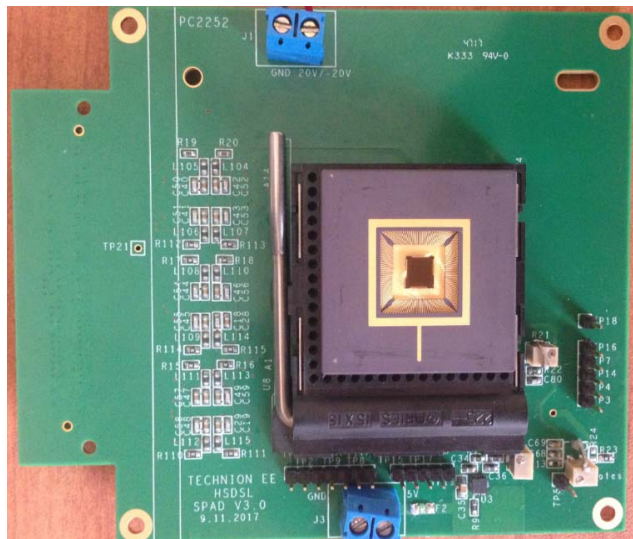
Fig. 3. Conceptual array operations at each frame end. The "LATCH" pulse stores the accumulated counts into the local memory (a), and then, the "RESET" pulse resets all counters for starting a new frame (b). The data is read out sequentially by selecting the appropriate address in a row-by-column addressing scheme (c).

256×256 pixels, with minor circuitry modifications. In future, the frame time may be reduced in order to increase the system's immunity to false alarms via oversampling and the pixel's FF could perhaps be increased as well (by reduction of the counter and latch sizes and also by the attachment of micro-lenses).

C. Summary of Pixel Properties

Measurement and elaboration on other properties of the pixel under study (such as photon detection efficiency, dark count rate and other SPAD detector parameters), detailed pixel content descriptions, and the pixel's operation principle, may all be found in [39]. The SPAD actual active area diameter is

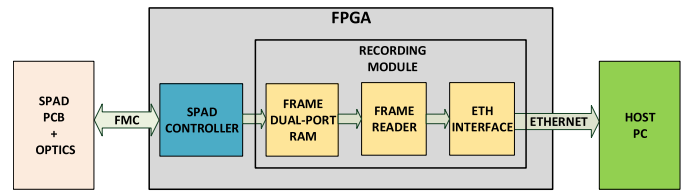Fig. 4.   The packaged imager chip mounted on the mezzanine board.

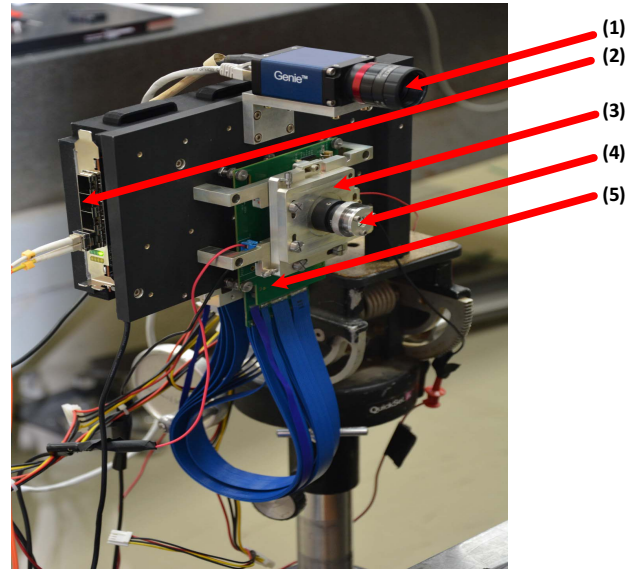Fig. 5.   Block diagram of the muzzle flash detection system.

Fig. 6.   The implemented imager used for the field experiments – (1) Commercial high-resolution CMOS imager for the spatial synchronization with SPAD imager, (2) FPGA board used for the communication with SPAD imager, (3) Specially-designed opto-mechanical system for the SPAD imager, (4) Narrowband optical filter (769nm±5nm), (5) CMOS SPAD imager placed on the mezzanine board.

11.5 μm. The layout of the SPAD device is 25 μm diameter. Accordingly, the FF is 21%. The FF of the pixel with auxiliary circuitry is 3.5%. The FF should be increased in the next imager generation.

D. Imager Architecture

The pixel described in [39] is a basic building-block of the SPAD array. The selected imager architecture makes possible the fully parallel operation of all pixels, thus allowing image acquisition at very high frame rates. 64 identical pixels form the one row and 64 identical rows form the full array. Figure 3 depicts the principal architecture of the imager. The memory is read out via 8-bit buses running vertically along the columns, while control signals (e.g., column and row selections and power supply lines) travel horizontally. The output of the imager is a 64-bit data bus. Frame acquisition begins with a global "RESET" pulse, sent to all array pixels, which resets every pixel's internal counter. During the integration frame time, all 4096 pixels work in photon-counting mode and operate independently; each counter accumulates the number of photons (and dark counts) detected by the corresponding SPAD.

At the end of the frame, a global "LATCH" pulse is applied to all pixels to store each pixel's photon count to its pixel memory register (Fig. 3(a)). After a very short time delay (20 ns) to avoid time overlapping between consecutive commands, a new "RESET" pulse resets all pixel counters, marking the beginning of a new frame (Fig. 3(b)). The stored data are available during the whole next frame before a new "LATCH" pulse updates the memory with the new frame data. The data of the previous frame is read out during the acquisition of the new frame (in a pipelined "integrate-while-read" manner). This pipelining causes a fixed latency of one frame in the information reaching the FPGA.

The array global electronics sequentially address all pixels, as shown in Fig. 3(c). The slow row address selects one row continuously, while the fast column address scans all columns and selects, in each incremental step, 8 columns simultaneously. Such an acquisition scheme corresponds to the electronic global shutter, which avoids any image artifacts or problems related to rolling shutter operation.

If the imager's performance makes it possible, the frame time can be reduced. A reduction of the frame time can be beneficial in terms of increased system's immunity to false alarms due to the detection process repetition; also, the smaller dynamic range (and the resultant lower-resolution counter) will allow a FF increase.

The minimal frame time limit is set by the time required to read out an entire frame. This time is dictated by the process' parasitic elements, namely its capacitive loads and the internal buffers' and output drivers' strength.

The simulated post-layout worst-case delay was about 19 ns. This delay was from the rise time of the "LATCH" signal to the most distant pixel's output bit rise time, taking place along a path loaded by an expected capacitance of 10 pF. In the real-life integrated system, the minimal acquisition time of the 8-pixel bundle was measured as significantly longer (about 50 ns excluding the "LATCH" and "RESET" pulses' time). This difference can be explained by the unexpectedly high capacitive load of the sensor's package, socket, and the relatively long line connecting the sensor to the FPGA.
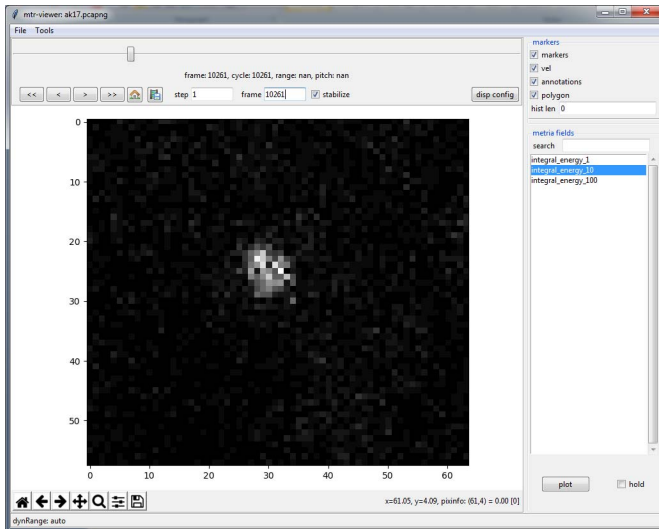
Fig. 7. The real muzzle flash detection image captured by the developed SPAD imager at 15 kHz sampling frequency.

The packaged chip was mounted on a dedicated mezzanine board, which connected the SPAD imager to the FPGA. This assembly is presented in Figure 4. Additionally, the mezzanine board provided the image sensor with its required power supplies.

IV. MUZZLE FLASH DETECTION SYSTEM

The packaged imager in Figure 4 was integrated, along with an FPGA, in a system that was tested in field experiments. The conceptual system block diagram is presented in Figure 5.

The electrical interface with the SPAD imager was implemented in FPGA. FPGA was selected for this purpose due to the lower power consumption relative to other options. The better power efficiency is achieved by using the FPGA to construct a spatial-computing solution, whereby the data flows through the computing elements and gets processes, similarly to an assembly line rather than a Von Neumann Processor-Memory architecture. While not critical for the currently included processing, this will become so in the future, as we include more sophisticated signal processing for improved quality, signal source characterization and other purposes. The FPGA interfaced with host-based human-machine interface (HMI) software that managed the operation of the SPAD imager and allowed control, configuration and recording of the sensor's output data. The host PC and the FPGA were connected via Ethernet. The FPGA design is comprised of SPAD controller and recording module. The SPAD controller is responsible to control the RESET and the LATCH signals and address bus. The recording module receives the frame data, stores the full frame into Block RAM, and after the frame is stored, it is transmitted using Ethernet interface to the Host PC. The imager continuously received and recorded shooting events at a sampling frequency of 15 kHz inside its field of view. The system was mechanically attached to an off-the-shelf lens and a narrowband spectral optical filter via a dedicated opto-mechanical interface, which also prevented

stray light from entering the SPAD's optical channel. The system was mounted on a tripod, and was attached to an off-the-shelf color camera, which was bore-sighted to the SPAD sensor and helped in the orientation of the system in the scene. The full system is presented in Figure 6.

As mentioned earlier, the system was tested in field experiments whose purpose was to prove the feasibility of the concept. During these experiments, the imager recorded AK-47 firing events inside its field-of-view. The muzzle flash was spread over two pixels to decrease a "blind" spots probability. A background photon counts for 2.5 mrad pixel's FOV during the sampling time is about 20 for ground in sunlight clutter. An example of a real AK-47 muzzle flash image, which was captured during the field experiment by the SPAD imager described herein, is presented in Figure 7.

V. CONCLUSION

We presented the design of a 64×64 CMOS SPAD imager for gun muzzle flash detection, fabricated in a standard low-cost 0.18 μm CMOS technology. The SPAD pixel consists of a SPAD detector and an 8-bit counter able to measure a light intensity by photon-counting. The pixel also includes pixel-level memories which allow fully parallel imaging in global shutter mode and store a 2-D intensity map of the previous acquired frame. This pixel is the building block of the SPAD imager, integrated in the SPAD camera. The full imager's array logic and circuit design considerations were presented. The imager was integrated with an FPGA, was opto-mechanically attached to an optical system with a field-of-view of $9° \times 9°$ and a narrowband spectral filter, and was controlled externally via HMI software. In addition, the real field experiment results captured at 15 kHz sampling frequency were presented. The results confirm the feasibility of gun muzzle flash online detection in the visible or NIR spectrum by uncooled silicon SPAD detectors in standard CMOS technology.

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